Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 46-82 as follows:

Listing of Claims:

1-45. (Cancelled)

46. (New) A delay-locked loop, comprising:

a ring oscillator operable to generate a plurality of tap clock signals, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to receive one of the tap clock signals from the ring oscillator and operable to generate a coarse enable signal responsive to receiving a selected number of periods of the received tap clock signal, the selected number of periods of the received tap clock signal being determined by a coarse delay control signal;

a fine delay circuit coupled to the ring oscillator to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals as a fine delay enable signal; and

an output circuit coupled to the coarse and fine delay circuits, the output circuit operable to generate a delayed clock signal responsive to the coarse and fine delay enable signals.

47. (New) The delay-locked loop of claim 46 further comprising a comparison circuit adapted to receive an input clock signal and the delayed clock signal, and coupled to the output circuit and the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and fine delay control signals.

48. (New) The delay-locked loop of claim 47 wherein the comparison circuit is operable to generate the coarse and fine delay control signals responsive to the relative phases of the delayed and input clock signals.

49. (New) The delay locked loop of claim 47 wherein the comparison circuit includes an input buffer adapted to receive the input clock signal and operable to generate a clock buffer signal.

50. (New) The delay-locked loop of claim 46 wherein the coarse delay circuit comprises a coarse reference register coupled to the comparison circuit and operable to develop a coarse reference count responsive to the coarse delay control signal.

51. (New) The delay-locked loop of claim 50 wherein the coarse delay circuit comprises:

a coarse delay counter coupled to the ring oscillator and the output circuit, the course delay counter developing a coarse delay count that is incremented responsive to the received tap clock signal from the ring oscillator, the coarse delay count being resetresponsive to the delayed clock signal; and

a comparator circuit coupled to the coarse reference register and the delay counter, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

52. (New) The delay-locked loop of claim 50 wherein each increment of the coarse reference count equals NxTPD, where N is the number of stages in the ring oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase difference between the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less

than NxTPD, and thereafter generates the fine delay control signal to select the tap clock signal from the ring oscillator that makes the determined phase difference less than or equal to TPD.

53. (New) The delay-locked loop of claim 46 wherein the fine delay circuit comprises a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the ring oscillator to receive a respective tap clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated.

54. (New) The delay-locked loop of claim 46 wherein the fine delay circuit comprises a shift register coupled to the comparison circuit to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the corresponding fine delay selection signal to apply the corresponding tap signal as the fine delay enable signal to the output circuit.

55. (New) The delay-locked loop of claim 46 wherein the output circuit comprises an AND gate.

56. (New) The delay-locked loop of claim 46 wherein the comparison circuit comprises:

a feedback delay line that generates a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal; and

a phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and fine delay control signals responsive to a detected phase between the feedback and input clock signals.

57. (New) The delay-locked loop of claim 56 wherein the phase detector detects the phase between rising-edges of the feedback and input clock signals.

58. (New) The delay-locked loop of claim 56 wherein the feedback delay comprises a first delay and a second delay, the first delay including a delay of an input buffer adapted to receive an external clock signal an develop the input clock signal in response to the external clock signal, and the second delay including a delay of the output circuit and a delay of an output buffer that receives the delayed clock signal and generates a synchronized clock signal in response to the delayed clock signal.

59. (New) A delay-locked loop, comprising:

a clock generator circuit operable to generate a plurality of clock signals, each clock signal having the same frequency and a respective phase relative to each other;

a coarse delay circuit coupled to the clock generator circuit to receive one of the clock signals and operable to generate a coarse enable signal responsive to a number of periods of the clock signal corresponding to a coarse delay control signal;

a fine delay circuit coupled to the clock generator circuit to receive the clock signals and operable responsive to a fine delay control signal to select one of the clock signals as a fine delay enable signal; and

an output circuit coupled to the coarse and fine delay circuits, the output circuit operable to generate a delayed clock signal responsive to the coarse and fine delay enable signals.

60. (New) The delay-locked loop of claim 59 wherein each clock signal has a progressively increasing phase relative to the other clock signals.

61. (New) The delay-locked loop of claim 59 further comprising a comparison circuit adapted to receive an input clock signal and the delayed clock signal, the comparison circuit operable to generate the coarse and fine delay control signals.

62. (New) The delay-locked loop of claim 61 wherein the comparison circuit is operable to generate the coarse and fine delay control signals responsive to the relative phases of the delayed and input clock signals.

63. (New) A delay-locked loop, comprising:

an oscillator operable to generate a plurality of clock signals, each clock signal having the same frequency and a respective phase relative to each other;

a coarse delay circuit coupled to receive one of the clock signals from the oscillator and operable to generate a coarse enable signal responsive to receiving a selected number of periods of the received clock signal, the selected number of periods being determined by a coarse delay control signal;

a rising-edge fine delay circuit coupled to the oscillator to receive the clock signals and operable responsive to a rising-edge fine delay control signal to select one of the clock signals as a rising-edge fine delay enable signal;

a falling-edge fine delay circuit coupled to the ring oscillator to receive the clock signals and operable responsive to a falling-edge fine delay control signal to select one of the clock signals and output the selected signal as a falling-edge fine delay enable signal; and

an output circuit coupled to the coarse delay circuit, the rising-edge delay circuit, and the falling-edge delay circuit, the output circuit generating a rising-edge of a delayed clock signal responsive to the coarse delay enable signal and the rising-edge fine delay enable signal going active, and the output circuit generating a falling-edge of the delayed clock signal responsive to the falling-edge fine delay enable signal going active.

64. (New) The delay-locked loop of claim 63 further comprising:

a comparison circuit adapted to receive an input clock signal and coupled to the output circuit to receive the delayed clock signal, and the comparison circuit being further coupled to the coarse delay circuit, the rising-edge delay circuit, and the falling-edge fine delay circuit, the comparison circuit operable to generate the coarse delay control signal, the rising-

edge delay control signal, and the falling-edge fine delay control signal in response to the relative phases of the delayed and input clock signals.

65. (New) The delay-locked loop of claim 63 wherein each increment of the coarse delay reference count equals NxTPD, where N is the number of stages in the oscillator and TPD is a propagation delay of each stage, and wherein the comparison circuit determines a phase difference between the rising and falling edges of the delayed and input clock signals and generates the coarse delay control signal to increment or decrement the coarse delay reference count when the determined phase difference is greater than NxTPD until the determined phase difference is less than NxTPD, and thereafter generates the rising-edge and falling-edge fine delay control signals to select respective clock signals, each selected clock signal making the corresponding phase difference less than or equal to TPD.

66. (New) The delay-locked loop of claim 63 wherein the coarse delay circuit comprises a coarse reference register coupled to the comparison circuit and operable to develop a coarse reference count responsive to the coarse delay control signal.

67. (New) The delay-locked loop of claim 63 wherein the coarse delay circuit comprises a coarse delay counter coupled to the oscillator and the output circuit, the course delay counter developing a coarse delay count that is incremented responsive to the received clock signal from the oscillator, the coarse delay count being reset responsive to the delayed clock signal.

68. (New) The delay-locked loop of claim 63 wherein the coarse delay circuit comprises a comparator circuit coupled to the coarse reference and delay counters, the comparator circuit activating the coarse delay enable signal responsive to the coarse delay count being equal to the coarse reference count.

69. (New) The delay-locked loop of claim 63 wherein each of the fine delay circuits comprises:

a plurality of transmission gates, each transmission gate including a first signal terminal coupled to the oscillator to receive a respective clock signal, a second signal terminal coupled to the output circuit, and a control terminal that receives a fine delay selection signal, each transmission gate coupling the first signal terminal to the second signal terminal in response to the fine delay selection signal being activated; and

a shift register coupled to the comparison circuit to receive the fine delay control signal and having a plurality of stages, each stage being coupled to the control terminal of a respective transmission gate, the shift register operable responsive to the fine delay control signal to shift an active bit into a selected one of the stages, the active bit activating the corresponding fine delay selection signal to apply the corresponding clock signal as the fine delay enable signal to the output circuit.

70. (New) The delay-locked loop of claim 63 wherein the output circuit comprises:

a first AND gate coupled to receive the coarse delay enable signal and the rising-edge fine delay enable signal on respective inputs, and operable to develop a rising-edge enable signal on an output;

a second AND gate coupled to receive the coarse delay enable signal and the falling-edge fine delay enable signal on respective inputs, and operable to develop a falling-edge enable signal on an output; and

a set-reset flip-flop having a set input coupled to the first AND gate and having a reset input coupled to the second AND gate, the flip-flop generating a rising-edge of the delayed clock signal on an output responsive to the set input and generating a falling-edge of the delayed-clock signal responsive to the reset input.

71. (New) The delay-locked loop of claim 63 wherein the comparison circuit comprises:

a feedback delay line that generates a feedback clock signal in response to the delayed clock signal, the feedback clock signal having a feedback delay relative to the delayed clock signal;

a rising-edge phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and rising-edge fine delay control signals responsive to a detected phase between rising-edges of the feedback and input clock signals; and

a falling-edge phase detector coupled to receive the feedback clock signal and the input clock signal, and operable to generate the coarse and falling-edge fine delay control signals responsive to a detected phase between falling-edges of the feedback and input clock signals.

72. (New) A computer system, comprising:

a data input device;

a data output device;

a processor coupled to the data input and output devices; and

a memory device coupled to the processor, the memory device comprising,

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a delay-locked loop coupled to at least the control circuit and adapted to receive an input clock signal, the delay-locked loop operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the delay-locked loop comprising,

a ring oscillator operable to generate a plurality of tap clock signals, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay circuit coupled to receive one of the tap clock signals from the ring oscillator and operable to generate a coarse delay count incrementing responsive to the received tap clock signal, the coarse delay circuit further operable to generate a coarse reference count in response to a coarse delay control signal and to activate a coarse delay enable signal responsive to the coarse delay count being equal to the coarse delay reference count, the coarse delay circuit resetting the coarse delay count responsive to a reset signal;

a fine delay circuit coupled to the ring oscillator adapted to receive the tap clock signals and operable responsive to a fine delay control signal to select one of the tap clock signals and output the selected signal as a fine delay enable signal; and

an output circuit coupled to the coarse delay circuit and the fine delay circuit, the output circuit generating a delayed clock signal responsive to the coarse and fine delay enable signals, and the delayed clock signal being applied as the reset signal to the coarse delay circuit to reset the coarse delay count.

73. (New) The computer system of claim 72 further comprising a comparison circuit adapted to receive the input clock signal and coupled to the output circuit to receive the delayed clock signal, the comparison circuit being further coupled to the coarse and fine delay circuits, the comparison circuit operable to generate the coarse and fine delay control signals in response to the relative phases of the delayed and input clock signals.

74. (New) A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of tap clock signals, each tap clock signal having a respective delay relative to one of the tap clock signals;

generating a coarse enable signal in response to one of the tap clock signals and a coarse delay control signal;

selecting one of the tap clock signals as a fine delay enable signal in response to a fine delay control signal; and

generating the delayed clock signal in response to the coarse and fine delay enable signals.

75. (New) The method of claim 74 wherein the coarse and fine delay control signals are generated responsive to an input clock signal and the delayed clock signal.

76. (New) The method of claim 75 wherein the coarse and fine delay control signals are generated responsive to the relative phases of the delayed and input clock signals.

77. (New) The method of claim 74 further comprising generating a coarse reference count responsive to the coarse delay control signal.

78. (New) The method of claim 74 further comprising:

generating a coarse delay count responsive to the clock generator signal and the delayed clock signal; and

resetting the coarse delay count responsive to the delayed clock signal.

79. (New) The method of claim 74 wherein the coarse delay enable signal is activated responsive to the coarse delay count being equal to the coarse reference count.

80. (New) A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of tap clock signals with one tap clock signal being designated as a clock generator signal, each tap clock signal having a period of predetermined duration;

generating a coarse enable signal having a period equal to a predetermined multiple of periods of the clock generator signal;

selecting one of the tap clock signals as a fine delay enable signal; and

generating a delayed clock signal responsive to the coarse and fine delay enable signals.

81. (New) The method of claim 80 further comprising generating a coarse and a fine delay control signal in response to an input clock signal and the delayed clock signal.

82. (New) The method of claim 81 wherein the coarse and fine delay control signals are generated responsive to the relative phases of the delayed and input clock signals.